

SUPPLEMENTARY AMENDMENT & RESPONSE UNDER 37 C.F.R. 1.116 - EXPEDITED PROCEDURE
Serial Number: 09/873,557
Filing Date: June 4, 2001
Title: FLOATING POINT MULTIPLY ACCUMULATOR
Assignee: Intel Corporation

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REMARKS

Claims 9 and 18 are amended, no claims are canceled, and no claims are added; as a result, claims 1-29 are now pending in this application.

In a previous response mailed on August 8, 2005, to which this response is intended as a supplement, claims 3, 4, 6, 11, 15, and 21-22 were rewritten in independent form to include all the limitations of the base claims and any intervening claims from which they previously depended, claim 10 was amended to depend from rewritten claim 11, and new claims 27-29 were added.

This response is a supplementary response to the previous response mailed on August 8, 2005, the previous response having been mailed along with a Request for Continued Examination. Attorney Robert Madden contacted Examiner Chat C. Do by telephone on August 9, 2005 in order to let him know of Applicant's intention to file this supplemental response. Applicant respectfully requests that the Examiner consider this supplemental response, including the additional amendments made in this supplemental response, along with the previously mailed response and the Request for Continued Examination, as responding to the Final Office Action mailed April 8, 2005.

§102 Rejection of the Claims

Claims 1-2, 8-9, 13-14, 18, and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wyland *et al.* (U.S. 6,205,462). Applicant does not admit that Wyland *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. § 1.131, to antedate Wyland *et al.* However, Applicant also urges that the claims 1-2 and 8 distinguish the reference, and therefore respectfully traverses the rejections of claims 1-2 and 8.

Independent claim 1

Claim 1 recites, "a floating point conversion unit to convert the product from the first exponent weight to a converted product with a second exponent weight." (emphasis added) Claims 2 and 8 depend from claim 1, and so include all of the elements recited in claim 1. Thus, the floating point conversion unit converts the product from a product having an exponent with a

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first exponent weight to a product with a second exponent weight. In contrast, Wyland *et al.* at column 4, lines 20-27, states, "Exponent sum 141 generated by adder 140 is the sum of two exponents E1 and E2 and hence represents the exponent of mantissa product 143. With the sum of exponents and final fixed point data format known, the necessary number of shifting places for the product of mantissas can be calculated and, therefore, shifter 144 can be designed accordingly to implement this shifting." Hence, Wyland *et al.* teaches an "exponent sum generated by adder 140," but fails to teach "a second exponent weight" for the exponent, and therefore fails to teach each of the elements of claim 1.

In response to this argument, the Final Office Action on page 7 submits that the case for converting the product from the first exponent weight to a converted product with a second exponent weight is seen whenever the input operands are integers and that the output of the exponent product of integers have to convert to a special floating-point exponent format as seen in Figure 1E.

However, Wyland *et al.* at column 4, lines 20-27 states, "Exponent sum 141 generated by adder 140 is the sum of two exponents E1 and E2 and hence represents the exponent of mantissa product 143. With the sum of exponents and final fixed point data format known, the necessary number of shifting places for the product of mantissas can be calculated and, therefore, shifter 144 can be designed accordingly to implement this shifting." However, there is no teaching in Wyland *et al.* that the exponent sum generated by adder 140 has a different exponent weight than either of the two exponents E1 or E2. Further, there is no teaching in Wyland *et al.* that the *product* of shifter 144 will have an exponent weight that is different from the exponent sum generated by adder 140. Hence, Wyland *et al.* discloses an "exponent sum generated by adder 140," but fails to teach to convert the product from the first exponent weight to a converted product with a second exponent weight as recited in claim 1 of the present application.

Independent claims 9 and 18.

Claim 9 as amended now recites, "wherein the mantissa shifter is configured to shift the product mantissa by a number of bit positions equal to a value of the least significant N bits of the product exponent, where N is a predetermined integer," and claim 18 as amended now recites, "wherein converting comprises: shifting a mantissa of the product by an amount

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equal to the value of the least significant N bits of the exponent of the product, where N is a predetermined integer; and zeroing the least significant N bits of an exponent of the product." Claims 13 and 14 depend from claim 9, and claim 20 depends from claim 18.

Claims 9 and 18 now follow the exact language of claims 11 and 21 respectively, except for the possibility of a number different from five. The cited art shows neither five nor any other predetermined integer number of bit-shift places. Further, both claims 11 and 21 are allowed except for a double-patenting rejection.

The specification supports these amendments to claims 9 and 18 wherein on page 7 at lines 8-10 the specification states, "For example, exponent path 312 ... sets the least significant five bits to zero...." [Emphasis Added]. Thus, five is an example; one skilled in the art would readily understand that any other number would operate in exactly the same manner to produce weights of other than 32. Thus, the amendments to claims 9 and 18 are supported in the specification.

Dependent claims 2, 8, and 13-14.

Claims 2 and 8 depend from claim 1, and so include all of the elements recited in claim 1. Claims 13 and 14 depend from claim 9, and claim 20 depends from claim 18. Thus, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 2-8, 13-14 and 20.

Summary

For the above and other reasons, Applicant urges that claims 1-2, 8-9, 13-14, 18, and 20 meet all the statutory requirements, and ought to be allowed. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 1-2, 8-9, 13-14, 18, and 20.

§103 Rejection of the Claims

Claims 12, 16-17, and 19 were rejected under 35 U.S.C. § 103(a) as being obvious over Wyland *et al.* (U.S. 6,205,462) in view of Dibrino *et al.* (U.S. 6,542,915). Applicant does not admit that either Wyland *et al.* or Dibrino *et al.* is prior art and reserves the right to antedate Wyland *et al.* and Dibrino *et al.* as provided for under 37 C.F.R. § 1.131.

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Claims 12 and 16-17 depend from claim 9, and therefore include all the elements of claim 9. Claim 19 depends from claim 18, and therefore includes all the elements of claim 18. As noted above, claim 9 recites, "an exponent conversion unit coupled to the output of the exponent summer, to convert the product exponent to a second weight," and claim 18 recites, "converting the product to have a different least significant bit weight exponent field." In addition, claims 9 and 18 include the additional elements added by amendment as discussed above.

As stated in connection with claims 1, 9, and 18 above, Wyland *et al.* fails to teach or suggest these elements. Further, Applicant does not find in Dibrino *et al.* these elements missing from Wyland *et al.* Instead, Dibrino *et al.* at column 2, lines 62-64, states, "FIG. 1 illustrates a typical floating-point pipeline. This diagram shows the 'Mantissa' dataflow only (the exponent dataflow logic is not shown)," and at column 6, lines 63-66, "FIG. 8 represents pipeline stage 2 of the floating-point pipeline of FIG. 1 with the prior art two-input LZA block 101 replaced by the new 'high-order' LZA 801, with N=5 (A five-input LZA)," and at column 7, lines 4-5, "Elements 804, 807, 808, 809, 810 operate similarly to blocks 104, 107, 108, 109, 110." Hence, Dibrino *et al.* also fails to teach or suggest each of the elements as recited in claims 9 and 18.

Thus, neither Wyland *et al.* nor Dibrino *et al.*, either alone or in combination, teach or suggest each of the elements of claims 9 and 18, so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19.

For the above and other reasons, Applicant urges that claims 12, 16-17, and 19 meet all the statutory requirements, and ought to be allowed. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 12, 16-17, and 19.

Double Patenting Rejection

Claims 9-14, 16, and 18-26 were rejected under the judicially created doctrine of double patenting over claims 1, 3-6, 9, and 11-18 respectively of U.S. Patent No. 6,779,013.

Applicant does not admit that claims 9-14, 16, or 18-26 are obvious in view of U.S. Patent No. 6,779,013. Applicant believes these claims are patentable over claims 1, 3-6, 9, and 11-18 of U.S. Patent No. 6,779,013, and therefore has chosen not to submit a Terminal Disclaimer at this time to overcome the rejection. However, Applicant will reconsider the

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submission of a Terminal Disclaimer at a later time in light of allowances of claims 9-14, 16, and 18-26 except for the double patenting rejection.

Allowable Subject Matter

Claims 3-7 and 15 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 4, 6, and 15 have been rewritten in independent form. Claim 5 has not been rewritten in independent form, but depends from rewritten claim 4. Claim 7 has not been rewritten in independent form, but depends from rewritten claim 6. In addition, new claim 27 depends from rewritten claim 3, and new claim 28 depends from rewritten claim 15.

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Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6971 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 16 Aug 2005,

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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

Amy J. Moriarty

August 16, 2005
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